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Claims

[c1] 1. A method of manufacturing a semiconductor device, comprising the steps of:
providing a substrate;
forming a plurality of conductive structures over the substrate, wherein each conductive structure comprises a conductive layer and a cap layer over the conductive layer;
forming spacers on the sidewalls of the conductive structures;
forming a first dielectric layer over the substrate;
removing a portion of the first dielectric layer, a portion of the cap layer and the spacers between neighboring conductive structures to form a plurality of first openings;
forming a bottom plug in the first openings;
forming a second dielectric layer over the substrate;
forming a plurality of second openings in the second dielectric layer, wherein each second opening exposes a portion of the bottom plug, and the second opening has a critical dimension smaller than the open end of the first opening;
forming a top plug inside the second openings; and

forming a plurality of wire lines over the second dielectric layer so that the wire lines and the top plugs are electrically connected.

[c2] 2. The method of claim 1, wherein the first opening has a funnel shape.

[c3] 3. The method of claim 2, wherein the step of forming a funnel shape opening comprises performing an anisotropic etching operation to remove a portion of the first dielectric layer, a portion of the cap layer and the spacers between neighboring conductive structures, moreover, the anisotropic etching process uses an etchant with a high etching selectivity between the first dielectric layer and the cap layer/the spacers, a low etching rate for the cap layer/spacer layer but a high etching rate for the first dielectric layer.

[c4] 4. The method of claim 1, wherein after removing a portion of the first dielectric layer, a portion of the cap layer and the spacer to form the first openings between neighboring conductive structures, the first openings expose the shoulder section of the conductive layers, and after forming the first openings, further comprises:
removing the shoulder section of the conductive layer to form a shoulder recess; and
forming a liner layer on the sidewalls of the first open-

ings.

[c5] 5. The method of claim 4, wherein the step of forming a liner layer on the sidewalls of the first openings comprises:
forming a liner material layer over the substrate to cover the first dielectric layer, the conductive structures and the sidewalls and bottom section of the first openings; and
performing an anisotropic etching of the liner material layer to form the liner layer on the sidewalls of the first openings.

[c6] 6. The method of claim 5, wherein material constituting the liner material layer is different from the second dielectric layer.

[c7] 7. The method of claim 4, wherein the step of forming the top plugs and the wire lines comprises:
forming a second conductive layer over the substrate to cover the second dielectric layer and fill the second openings, wherein the second conductive layer within the second opening forms the top plug; and
patterning the second conductive layer to form the wire lines.

[c8] 8. The method of claim 1, wherein the step for forming

the top plugs and the wire lines further comprises:
forming a second conductive layer over the substrate to cover the second dielectric layer and fill the second openings, wherein the second conductive layer within the second openings form the top plug; and
patterning the second conductive layer to form the wire lines.

[c9] 9. A method of manufacturing a semiconductor device, comprising the steps of:
providing a substrate;
forming a plurality of conductive structures over the substrate, wherein each conductive structure comprises a conductive layer and a cap layer over the conductive layer;
forming spacers on the sidewalls of the conductive structures;
forming a dielectric layer over the substrate;
removing a portion of the dielectric layer, a portion of the cap layer and the spacers between neighboring conductive structures to form a plurality of openings that exposes a shoulder section of the conductive layers;
removing the shoulder section of the conductive layers to form a shoulder recess;
forming a liner layer on the sidewalls of the openings; and

forming a conductive plug inside the openings.

[c10] 10. The method of claim 9, wherein the opening has a funnel shape.

[c11] 11. The method of claim 10, wherein the step of forming a funnel shape opening comprises performing an anisotropic etching operation to remove a portion of the dielectric layer, a portion of the cap layer and the spacers between neighboring conductive structures, moreover, the anisotropic etching process uses an etchant with a high etching selectivity between the dielectric layer and the cap layer/the spacers, a low etching rate for the cap layer/spacer layer but a high etching rate for the dielectric layer.

[c12] 12. The method of claim 9, wherein the step of forming a liner layer on the sidewalls of the openings comprises: forming a liner material layer over the substrate to cover the dielectric layer, the conductive structures and the sidewalls and bottom section of the openings; and performing an anisotropic etching of the liner material layer to form a liner layer on the sidewalls of the openings.

[c13] 13. The method of claim 12, wherein material constituting the liner material layer is different from the dielectric

layer.

[c14] 14. A semiconductor device, comprising:
a substrate;
a plurality of conductive structures formed on the substrate;
a plurality of bottom plugs set up between neighboring conductive structures and electrically connected to the substrate;
a liner layer set up between the neighboring conductive structures and the conductive bottom plugs;
a plurality of top plugs set up over the respective bottom plugs, wherein the junction portion of the bottom plug connected to the top plug has a critical dimension greater than the top plug;
a plurality of wire lines connected electrically to the respective top plugs; and
a dielectric layer set up between the conductive structure, between the bottom plugs and between the top plugs and between the wire lines.

[c15] 15. The semiconductor device of claim 14, wherein the bottom plug is a solid block with a funnel shape.

[c16] 16. The semiconductor device of claim 14, wherein the top plug is a solid block with a cylindrical shape.

[c17] 17. The semiconductor device of claim 14, wherein each conductive structure further comprises a conductive layer with a shoulder recess.

[c18] 18. A semiconductor device, comprising:
a substrate;
a plurality of conductive structures on the substrate with each conductive structure comprising a conductive layer and a cap layer, wherein the conductive layer of every pair of neighboring conductive structures has a recess shoulder;
a plurality of conductive plugs set up between neighboring conductive structures and electrically connected to the substrate; and
a liner layer set up between neighboring conductive structures and the conductive plugs.

[c19] 19. The semiconductor device of claim 18, wherein the conductive plug is a solid block with a funnel shape.